

EV633261932

Inventor: **Arup Bhattacharyya**

Title: **Computer Systems Utilizing High Performance Three-Dimensional TFT-Based CMOS Inverters**

Assignee: **Micron Technology, Inc.**

Serial No.: **10/760,087**

Filed: **January 14, 2004**

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

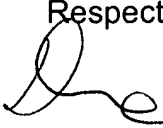
PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

The attached Form PTO-1449 is submitted in compliance with 37 CFR §1.56. Pursuant to FEDERAL REGISTER, Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art are attached. No admission is made regarding whether the listed references are prior art.

This Supplemental Information Disclosure Statement is being submitted pursuant to the Examiner's remarks in his 9/13/05 Office Action where he states that nine previously submitted articles were not completely readable and therefore were not initialed by him. Therefore, no fee is believed to be required for resubmitting the cited articles. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.


Citation of these references is respectfully requested.

Date: 11/28/05

Respectfully submitted,


David G. Latwesen, Ph.D.
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Form PTO-1859		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2473		SERIAL NO. 10/760,087	
				LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)			
				APPLICANT Arup Bhattacharyya			
				FILING DATE January 14, 2004		GROUP 2826	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AG						
	AH						
	AI						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AJ		King, T. et al., "A Low-Temperature ($\leq 550^\circ\text{C}$) Silicon-Germanium MOS Thin-Film Transistor Technology for Large-Area Electronics", IEDM Tech. Digest, 1991, pp. 567-570.				
	AK		Kuriyama, H. et al., "High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics", IEDM Tech. Digest, 1991, pp. 563-566.				
	AL		Kim, C.H. et al., "A New High-Performance Poly-Si TFT by Simple Excimer Laser Annealing on Selectively Floating a-Si Layer", IEDM Tech. Digest, 2001, pp. 751-754.				
	AM		Hara, A. et al., "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization", IEDM Tech. Digest, 2001, pp. 747-750.				
	AN		Gu, J. et al., "High Performance Sub-100 nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing", DRC Conf. Digest, 2002, pp. 49-50.				
	AO		Rim, K. et al., "Characteristics and Device Design of Sub-100 nm Strained SiN- and PMOSFETs", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 98-99.				
	AP		Park, J.S. et al., "Normal Incident SiGe/Si Multiple Quantum Well Infrared Detector", IEDM Tech. Digest, 1991, pp. 749-752.				
	AQ		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBT's", IEEE Elec. Dev. Lett., Vol. 18, No. 7, July 1997, pp. 333-335.				
	AR		Lu, N. et al., "A Buried-Trench DRAM Cell Using a Self-Aligned Epitaxy Over Trench Technology", IEDM Tech. Digest, 1988, pp. 588-591.				
EXAMINER		DATE CONSIDERED					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							